

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

Agere Yee 7

Application Number

10/148,068
TBA

Applicant(s)

Oceager P. Lee

Filing Date

12/29/2003
TBA

Group Art Unit

TBA 2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JSL	A	6,249,893 B1	6/19/2001	Rajsuman et al.	714	741	
JSL	B	6,484,280 B1	11/19/2002	Moberly	714	726	
JSL	C	6,519,711 B1	2/11/2003	Fischer et al.	714	30	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

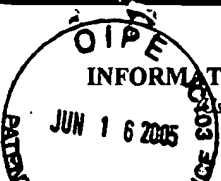
EXAMINER

James Sun Hing

DATE CONSIDERED

10-5-05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<div style="text-align: center;">  <p>INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p> </div>	Docket Number (Optional) 6002-104US	Application Number 10/748,068
	Applicant(s) Oceager P. Yee	
	Filing Date 12/29/2003	Group Art Unit 2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JSR		5,678,003	10/14/97	Jeffrey S. Brooks	714	34	
JSR		5,812,562	09/22/98	Sanghyeon Baeg	714	726	
JSR		6,385,742 B1	05/07/02	Graham Kirsch, et al.	714	39	
JSR		2002/0138801 A1	09/26/02	Laung-Terng Wang, et al.	714	729	

FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
JSR	GB 2 337 834 A	01.12.1999	GB	—	—	✓	
JSR	WO 03/065065 A1	07.08.2003		—	—	✓	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JSR	1	"Silicon Debug: Scan Chains Alone Are Not Enough" by Gert Jan van Rootselaar and Bart Vermeulen; ITC International Test Conference; 1999 IEEE, pages 892-902
JSR	2	"Hierarchical Data Invalidation Analysis for Scan-Based Debug on Multiple-Clock System Chips" by Sandeep Kumar Goel and Bart Vermeulen; ITC International Test Conference; 2002 IEEE, pages 1103-1110

EXAMINER <i>James Sun</i>	DATE CONSIDERED <i>10-5-05</i>
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6002-104US

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*EXAMINER
INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

"Test and Debug Techniques for Multiple Clock Domain SoC Devices" by Ross R. Youngblood, Electronics Manufacturing Technology Symposium, 2004 IEEE, pages 202-205

EXAMINER

James P. Smith

DATE CONSIDERED

10-5-05

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